REMARKS

Claims 1 through 23 are pending in this application. Claims 1, 7, 9, 14 and 16 are amended herein. Claims 6, 13, 22 and 23 are cancelled.

Claims 1 through 23 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Heidel et al., U.S. Patent No. 6,230,290 (Heidel) and Kablanian et al., U.S. Patent No. 5,764,878. This rejection is respectfully traversed in view of the following comments and amendments made herein.

Kablanian teaches a particular Built-In Self-Testing (BIST) and Built-In Self-Repair (BISR) mechanism. When the memory is powered up, a self-test routine begins which determines the presence of defective row memory lines or faulty Input/Output (I/O) memory blocks. Defective row memory lines are replaced by redundant functional row memory lines and an addressing table is changed to reflect the substitution. Defective I/O memory blocks are replaced in a similar fashion.

Even taken at its broadest, Kablanian only teaches subject matter that is general prior art, and also noted as such in the present application. Applicants do not claim to have invented BIST and BISR. Both are known in the art. The Applicants have, however, claimed a technique of stressing memory cells of a semiconductor memory during power-on operations that determines which memory cells will fail under stressed environmental and operating conditions. These conditions are those that are most likely to be encountered during normal operation. The stress clock signal is not, however, used during normal memory access operations. This is an important distinction between what is now claimed, and the teachings of the prior art. The prior art, in essence, is teaching a way of identifying conditions at which a memory will ultimately operate. If the memory passes at the given test frequency, the chip is rated for use in those specified conditions. However, the stress clock will not be used during normal operating conditions, and this limitation has been added to the independent claims.

The claimed invention also defines replacing both defective and so-called weak memory cells (those cells that function properly at moderate environmental conditions but

which fail when, for example, environmental conditions worsen (e.g. the temperature rises)) prior to operational use of the memory. This testing and repair occurs each time the memory is powered up and insures that only memory cells that are robust and likely to survive environmental stress are used in the memory during operation.

Heidel teaches a method of BIST that tests the memory cells at increasing stress levels until failure occurs. The test parameters that can be altered are at least temperature, voltage and timing. Tests are repeated at varying stress levels to determine the maximum operating speed of a particular memory. As noted above, these levels are those that, if passed, will serve to operate the memory cells. The teachings of Heidel, therefore, do not provide motivation to test at a stress level that will *not* be used during normal operation, as it is Heidel's goal to find actual *functional operating levels* of the memory cells using stressed functional conditions.

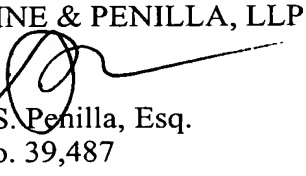
As amended, each independent claim recites that the memory is tested with a stress test clock that has a predetermined frequency greater than the internal clock signal. The internal clock signal is the functional signal that will be used during normal operations. The predetermined frequency that is greater than the internal clock signal is designed to simulate the functioning of the memory array under stressed environmental and operating conditions. The stress clock, as claimed, is used initially at the powering up of the memory. Memory cells that fail under these conditions are replaced by reserve redundant cells that can function under these stress conditions. In this manner, the memory can function without being interrupted by failure of weak cells during actual operations. Again, the test methods described in Heidel are not used in an operational environment. Rather, they are adjuncts to preparing the memories for sale by grading the memories into various performance classes.

It is respectfully submitted that the teachings of Heidel alone or combined with the teachings of Kablanian fail to render the now amended claims obvious. For at least the forgoing reasons and amendments, the Applicants respectfully request the Office to withdraw the Section 103 rejection.

A Notice of Allowance is therefore respectfully requested.

If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6903. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No ARTCP031). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE & PENILLA, LLP



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